Sequencer and Method of Selectively Inhibiting Clock Signals to Execute Reduced Instruction Sequences in a Re-Programmable I/O Interface

Abstract of the Disclosure

A sequencer executes instructions based on a function clock signal to perform I/O functions in a serial peripheral interface based on a source clock signal. The function clock signal has a frequency of two times the frequency of the source clock signal. A function clock generator generates the function clock signal and operatively selects the instruction to be decoded. The instruction selectively forces the frequency of the function clock signal to be equal to the frequency of the source clock signal during the duration of that function clock signal during which the predetermined instruction is decoded to execute a single instruction during the source clock signal, to advantageously repeat the execution of the instruction without consuming clock cycles.

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